UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/734,195 | 12/15/2003 | Kwun Yao Ho | 025796-00014 | 4785 |

7590 03/09/2006

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 400
1050 Connecticut Avenue
Washington, DC 20036-5339

| EXAMINER | |
|---|---|
| BRYANT, DELORIS S | |
| ART UNIT | PAPER NUMBER |
| 2813 | |

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5/1

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/734,195 | HO ET AL. | |
| | Examiner | Art Unit | |
| | Deloris Bryant | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's response to non-final rejection dated December 5, 2005 is acknowledged.

### *Drawings*

Amendment to claim 12 in response to examiner's objection is acknowledged.

### *Specification and Claim Objections*

Amendment to the specification and claim 3 in response to examiner's objection is acknowledged.

### *Claim Rejections - 35 USC § 112*

Amendment to claim 8 in response to examiner's rejection under 35 U.S.C. 112, second paragraph is hereby acknowledged.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and in further view of Watanabe et al (US 6,791,193). Juskey discloses a multichip module structure comprising a semiconductor substrate (Fig. 5; 512) having a first surface and a second surface ("top" and "bottom" of 512, respectively); an insulating layer on said first surface (Fig. 5; 520) and a plurality of chips (Fig. 5; 522 and 532), however, does not discloses a multilayer interconnection structure. Wantanabe does teach an interconnection structure with a third surface having a plurality of first bonding pads (Fig. 10; 17a-f) and a fourth surface having a plurality of second bonding pads (Fig. 10; 14a-f) and a plurality of third bonding pads (Fig. 10; 7a-f) on said second surface and connecting to said conductive plus respectively. Neither Juskey or Wantanabe teach a plurality of conductive plugs penetrating the substrate and insulating layer and electrically connecting to said second bonding pads. Koyanagi, however, does teach a substrate (Fig. 1; 11) whose upper and lower surfaces are covered with an insulator film (Fig. 1; 12 and 13). Koyanagi also teaches that conductive plugs (Fig. 1; 15) do penetrate the substrate (Fig. 1; 11) and insulating layer (Fig. 1; 12 and 13) and electrically connect to bonding pads (Fig. 1; 16 and 17). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to combine the interconnection structure of Wantanabe and the teaching of Koyanagi with the teaching of Juskey. One would have been motivated to so modify Juskey to achieve an improvement in the packaging operation efficiency.

Claims 2-3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and Watanabe et al (US 6,791,193) and in further view of Hayasaka et al (US 6,809,421). Juskey along with Koyanagi and Watanabe discloses the claimed invention as set forth above with respect to claim 1. However, Juskey, Koyanagi and Watanabe do not teach a multilayer interconnection structure includes at least one integrated circuit device (claim 2); that the semiconductor substrate has a thickness between 10-500 micron (claim 3); and that the first and second multichip module structure has the same structure (claim 11). Hayasaka et al discloses a multilayer interconnection structure includes at least one integrated circuit device (col. 9 – col. 10, line 67 and lns 1-2, respectively) and that the hole in the silicon substrate is 100 μm (col. 12, lns 27-30), which indicated that the thickness of the substrate is at least 100 μm thick which falls within the range indicated by the applicant. Hayasaka also discloses that multiple structures can be of the same structure (col. 11, lns 11-13; see fig. 4 and 5). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the structure taught by Hayasaka to produce a device that is small in area, simple in structure and small in thickness.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and in further view of Watanabe et al (US 6,791,193). Juskey along with Koyanagi and Watanabe discloses the claimed invention as set forth above with respect to claim 1.

Furthermore, Juskey teaches that a multi-chip module includes a passive and active chip (col. 5, lns 59-60). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide an active and passive chip to be included in the multi-chip module structure for the benefit of using a much less costly technique.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and Watanabe et al (US 6,791,193) and in further view of Taniguchi et al (US 6,404,062). Juskey teaches that a multi-chip module includes a passive and active chip (col. 5, lns 59-60). Taniguchi teaches a flip-chip mounting process (col. 1, lns 41-51). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the flip-chip mounting process of Taniguchi et al with the passive and active chips from Juskey so that connecting reliability can be ensured.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and in further view of Watanabe et al (US 6,791,193). Juskey teaches that a multi-chip module includes a passive and active chip (col. 5, lns 59-60). Furthermore, Watanabe teaches structure that includes third bonding pads. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to combine the chips of Juskey with structure taught by Watanabe so that electric signal can be derived from the pad and sent to the rest of the device.

Claims 8-9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and Watanabe et al (US 6,791,193) and in further view of Peterson et al (US 6,809,413). Juskey along with Koyanagi and Watanabe discloses the claimed invention as set forth above with respect to claim 1 but do not teach a first chip mounted on a second surface by flip-chip type and second chip electrically connecting and stacking on a backside of first chip. Peterson, however, does teach a chip (Fig. 3A; 100) attached to a second surface (Fig. 3A; 18) by flip-chip type and a second chip (Fig. 5; 102) connected to the backside of the first chip (col. 11, lns 62-67). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to mount the chips by flip-chip type because of the many benefits including increased packaging density, thinner package height and electrical circuit interconnection.

Regarding claim 10, Juskey along with Koyanagi, Watanabe and Peterson discloses the claimed invention as set forth above with respect to claim 1 and 8. Furthermore, Juskey teaches that a multi-chip module includes a passive and active chip (col. 5, lns 59-60). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide an active and passive chip to be included in the multi-chip module structure for the benefit of using a much less costly technique.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al (US 6,356,453) in view of Koyanagi (US 2005/0029643) and Watanabe et al (US

6,791,193) and in further view of Katagiri et al (US 2003/0111737). Juskey along with Koyanagi and Watanabe discloses the claimed invention as set forth above with respect to claim 1 but do not teach that the MCM structure is electrically connected with a package substrate. Katagiri does teach a MCM structure connected with a package substrate (Fig. 2; 1). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to take the package substrate of Katagiri and combine it with the teachings of Juskey along with Koyanagi and so that connecting reliability can be ensured and permitting reduction cost of the manufacturing of the MCM.

### *Response to Amendment*

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-0237. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dsb

CARL WHITEHEAD JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800